ESP32-C61

Hardware Design Guidelines

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This document provides guidelines for the ESP32-C61 SoC.

Schematic Checklist	PCB Layout Design	Download Guidelines	Resources

Chapter 1

Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32c61/index.html

1.1 About This Document

1.1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-C61 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif ' s standards. The guidelines are intended for hardware and application engineers.

The document assumes that you possess a certain level of familiarity with the ESP32-C61 SoC. In case you lack prior knowledge, we recommend utilizing this document in conjunction with the ESP32-C61 Series Datasheet.

1.1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32c61/index.html

1.2 Product Overview

ESP32-C61 is a system on a chip that integrates the following features:

- Wi-Fi 6 (2.4 GHz band)
- Bluetooth® 5 (LE)
- High-performance 32-bit RISC-V single-core processor
- Multiple peripherals
- Built-in security hardware

Powered by 40 nm technology, ESP32-C61 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-C61 include:

- Smart Home

- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

For more information about ESP32-C61, please refer to ESP32-C61 Series Datasheet.

Note: Unless otherwise specified, "ESP32-C61" used in this document refers to the series of chips, instead of a specific chip variant.

1.3 Schematic Checklist

1.3.1 Overview

The integrated circuitry of ESP32-C61 requires only 30 electrical components (resistors, capacitors, and inductors) and a crystal, as well as an SPI flash (in-package or off-package). The high integration of ESP32-C61 allows for simple peripheral circuit design. This chapter details the schematic design of ESP32-C61.

The following figure shows a reference schematic design of ESP32-C61. It can be used as the basis of your schematic design.

Any basic ESP32-C61 circuit design may be broken down into the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash and PSRAM*
- *Clock source*
- *RF*
- *UART*
- *Strapping pins*
- *GPIO*
- *ADC*
- *SPI*
- *SDIO*
- *USB*

The rest of this chapter details the specifics of circuit design for each of these sections.

1.3.2 Power Supply

The general recommendations for power supply design are:

- When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add an ESD protection diode and at least 10 µF capacitor at the power entrance.

More information about power supply pins can be found in ESP32-C61 Series Datasheet > Section *Power Supply*.

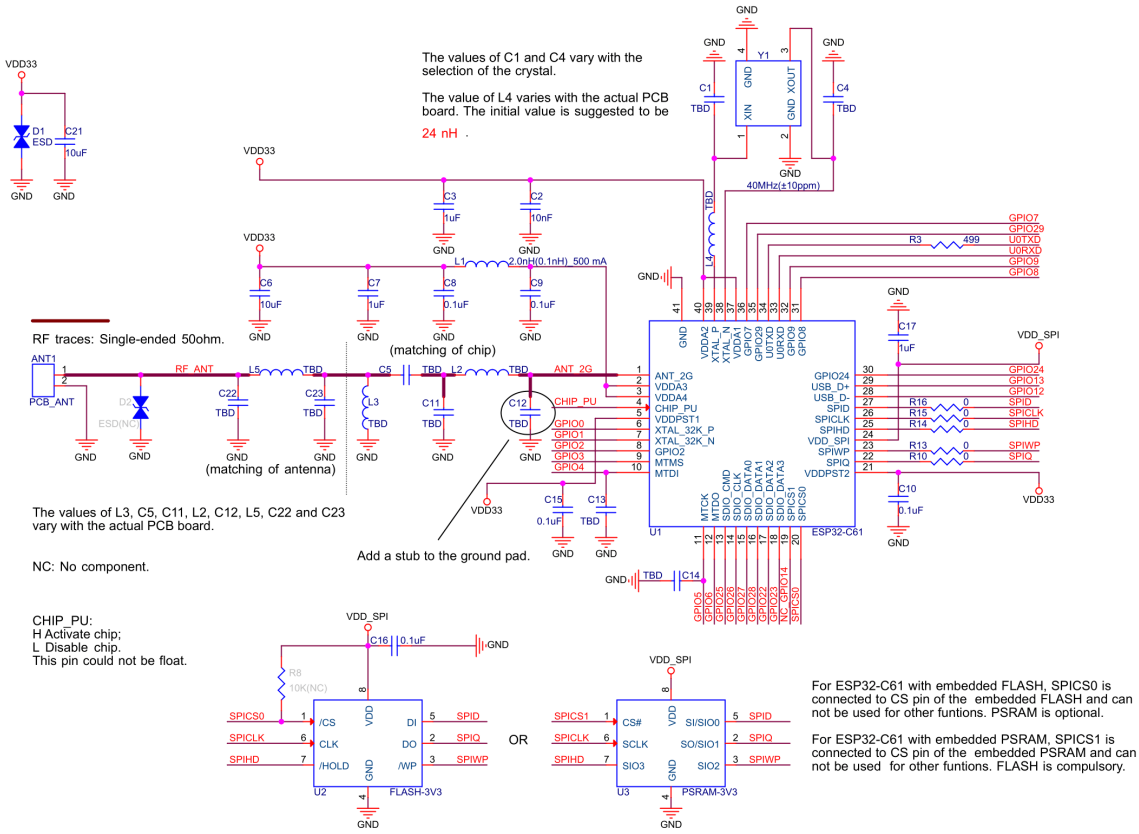
The values of C1 and C4 vary with the selection of the crystal.
The value of L4 varies with the actual PCB board. The initial value is suggested to be 24 nH .
RF traces: Single-ended 50ohm.
(matching of chip)
(matching of antenna)
The values of L3, C5, C11, L2, C12, L5, C22 and C23 vary with the actual PCB board.
NC: No component.
Add a stub to the ground pad.
CHIP_PU:
H Activate chip;
L Disable chip.
This pin could not be float.
For ESP32-C61 with embedded FLASH, SPICS0 is connected to CS pin of the embedded FLASH and can not be used for other funtions. PSRAM is optional.
For ESP32-C61 with embedded PSRAM, SPICS1 is connected to CS pin of the embedded PSRAM and can not be used for other funtions. FLASH is compulsory.
OR
40MHz(±10ppm)
ESP32-C61
FLASH-3V3
PSRAM-3V3

Fig. 1: ESP32-C61 Reference Schematic

Digital Power Supply

ESP32-C61 has pin5 VDDPST1 and pin30 VDDPST2 as the digital power supply pin(s) working in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 µF decoupling capacitor close to the pin(s).

Pin VDD_SPI (pin23) can serve as the power supply for the external device at 3.3 V (typical value), provided by VDDPST2 via R_{SPI}. Therefore, there will be some voltage drop from VDDPST2. When the VDD_SPI outputs 3.3 V, it is recommended that users add a 1 µF capacitor close to VDD_SPI.

VDD_SPI can be connected to and powered by an external power supply.

When not serving as a power supply pin, VDD_SPI can be used as a regular GPIO.

It is recommended to use the VDD_SPI to power the in-package or off-package flash/PSRAM.

Attention: When using VDD_SPI as the power supply pin for the in-package flash/PSRAM or external 3.3 V flash/PSRAM, considering the voltage drop mentioned above, VDDPST2 should be 3.0 V or above, so as to meet the requirements of flash/PSRAM's working voltage.

Analog Power Supply

ESP32-C61's VDDA1 to VDDA4 pins are the analog power supply pins, working at 3.0 V ~ 3.6 V.

For VDDA3 and VDDA4, when ESP32-C61 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 µF capacitor to the power rail, which can work in conjunction with the 1 µF capacitor(s) or other capacitors.

It is suggested to add an extra 10 µF capacitor at the power entrance. If the power entrance is close to VDDA3 and VDDA4, then two 10 µF capacitors can be merged into one.

Add an LC circuit on VDDA3 and VDDA4 power rails to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA and above.

For the remaining capacitor circuits, please refer to *ESP32-C61 Reference Schematic*.

1.3.3 Chip Power-up and Reset Timing

ESP32-C61's CHIP_PU pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-C61 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of (–0.3 ~ 0.25 × VDDPST1) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

Figure *ESP32-C61 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-C61.

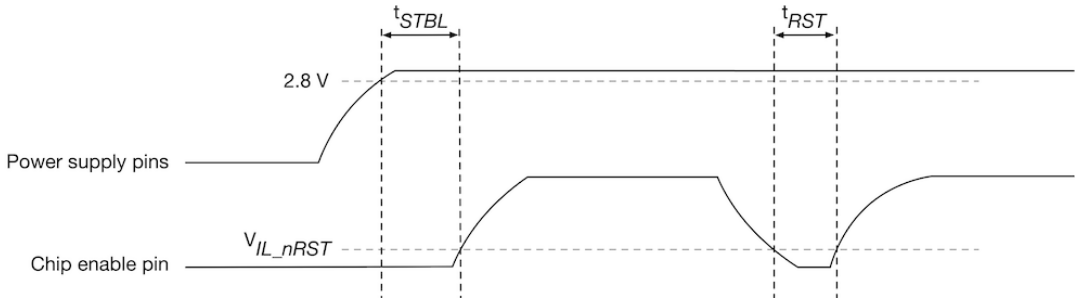

Fig. 2: ESP32-C61 Power-up and Reset Timing

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (µs)
t_{STBL}	Time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	50

Attention:

- CHIP_PU must not be left floating.
- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 µF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
  - Slow power rise or fall, such as during battery charging.
  - Frequent power on/off operations.
  - Unstable power supply, such as in photovoltaic power generation.

  Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:
  - Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
  - Implementing reset functionality through a button or the main controller.

1.3.4 Flash and PSRAM

ESP32-C61 requires in-package or off-package flash to store application firmware and data. In-package PSRAM or off-package PSRAM is optional.

In-Package Flash and PSRAM

The tables list the pin-to-pin mapping between the chip and in-package flash/PSRAM. Please note that the following chip pins can connect at most one flash and one PSRAM. That is to say, when there is only flash in the package, the pin occupied by flash can only connect PSRAM and cannot be used for other functions; when there is only PSRAM, the pin occupied by PSRAM can only connect flash; when there are both flash and PSRAM, the pin occupied cannot connect any more flash or PSRAM.

Table 2: Pin Mapping Between Chip and Off-Package Flash for ESP32-C61[1]

Pin No	Pin Name	Single SPI flash	Dual SPI flash	Quad SPI flash
26	SPICLK	CLK	CLK	CLK
20	SPICS0[2]	CS#	CS#	CS#
27	SPID	MOSI	SIO0[3]	SIO0
22	SPIQ	MISO	SIO1	SIO1
23	SPIWP	WP#		SIO2
25	SPIHD	HOLD#		SIO3

Table 3: Pin Mapping Between Chip and Off-Package PSRAM for ESP32-C61[4]

Pin No	Pin Name	Single SPI PSRAM	Quad SPI PSRAM
26	SPICLK	CLK	CLK
19	SPICS1[5]	CE#	CE#
27	SPID	SI[6]	SIO0
22	SPIQ	SO[7]	SIO1
23	SPIWP		SIO2
25	SPIHD		SIO3

Off-Package Flash and PSRAM

To reduce the risk of software compatibility issues, it is recommended to use flash and PSRAM models officially validated by Espressif. For detailed model selection, consult the sales or technical support team. It is recommended to add zero-ohm resistor footprints in series on the SPI communication lines as shown in Figure *ESP32-C61 Reference Schematic*. These footprints provide flexibility for future adjustments, such as tuning drive strength, mitigating RF interference, correcting signal timing, and reducing noise, if needed.

1.3.5 Clock Source

ESP32-C61 supports two external clock sources:

- *External crystal clock source (Compulsory)*

[1] An off-package flash can only be connected if the chip variant does not have in-package flash.
[2] SPICS0 is used to access flash
[3] SIO: Serial Data Input and Output
[4] An off-package PSRAM can only be connected if the chip variant does not have in-package PSRAM. If PSRAM is not connected, these pins cannot be used as GPIO pins.
[5] SPICS1 is used to access PSRAM
[6] SI: Serial Data Input, equivalent to MOSI
[7] SO: Serial Data Output, equivalent to MISO

- *RTC clock source (Optional)*

External Crystal Clock Source (Compulsory)

The ESP32-C61 firmware only supports 40 MHz crystal.

The circuit for the crystal is shown in Figure *ESP32-C61 Schematic for External Crystal*. Note that the accuracy of the selected crystal should be within ±10 ppm.

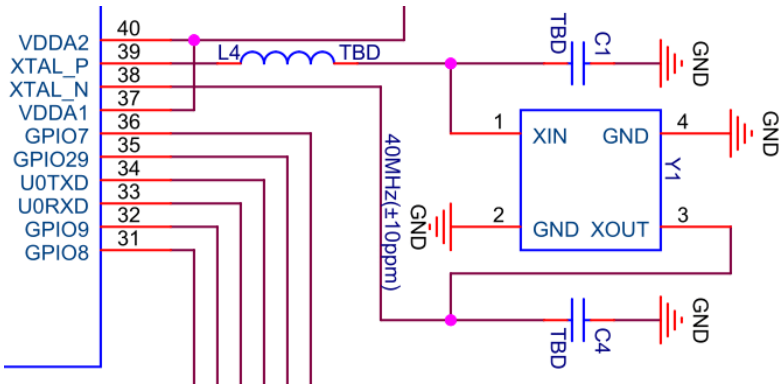

Fig. 3: ESP32-C61 Schematic for External Crystal

Please add a series component on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C2 can be determined according to the formula:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C2 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.

- When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
- When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
- External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

Note:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ±10 ppm, unstable performance within the operating temperature range, etc) may lead to the malfunction of ESP32-C61, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

RTC Clock Source (Optional)

ESP32-C61 supports an external 32.768 kHz crystal to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

Figure *ESP32-C61 Schematic for 32.768 kHz Crystal* shows the schematic for the external 32.768 kHz crystal.

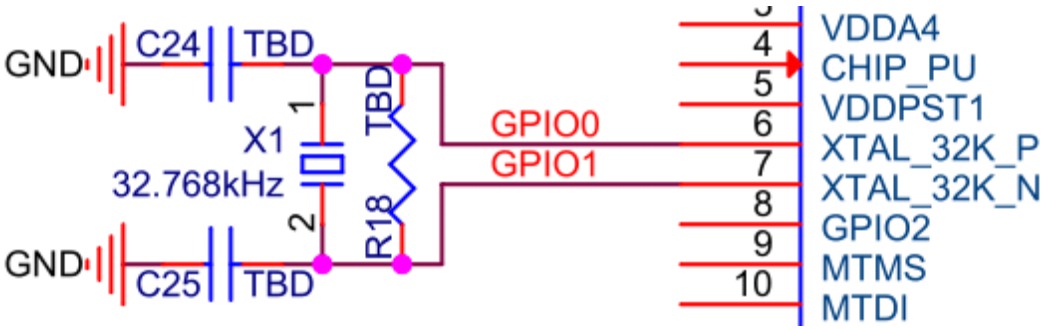

Fig. 4: ESP32-C61 Schematic for 32.768 kHz Crystal

Please note the requirements for the 32.768 kHz crystal:

- Equivalent series resistance (ESR) ≤ 70 kΩ.
- Load capacitance at both ends should be configured according to the crystal's specification.

The parallel resistor R is used for biasing the crystal circuit (5 MΩ < R ≤ 10 MΩ).

The resistor must be populated.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

1.3.6 RF

RF Circuit

ESP32-C61's RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. A CLCCL structure is preferred.
  - The CLCCL structure forms a bandpass filter, which is mainly used to adjust impedance points, suppress high-frequency harmonics, and suppress low-frequency noise.
  - The RF matching circuit is shown in Figure *ESP32-C61 Schematic for RF Matching*.
- For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.
- It is recommended to include ESD protection devices for the antenna to mitigate electrostatic interference.

Note: If you plan to apply for FCC/NCC certification, it is recommended to reserve capacitors to ground on GPIO4 and GPIO5 to effectively suppress harmonic interference. For customers not involved in such certifications, this is not necessary. If using the ANT2 of the ESP32-C61-WROOM-1U module, please add a CLC circuit at the ANT2 pin to suppress low-frequency noise.

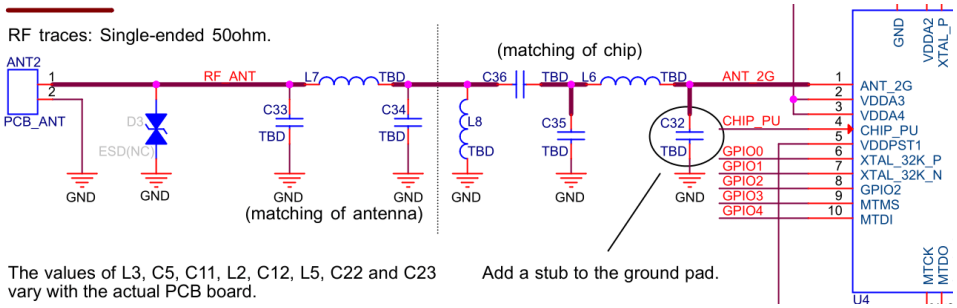

Fig. 5: ESP32-C61 Schematic for RF Matching

RF Tuning

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning.

Figure *ESP32-C61 RF Tuning Diagram* shows the general process of RF tuning.

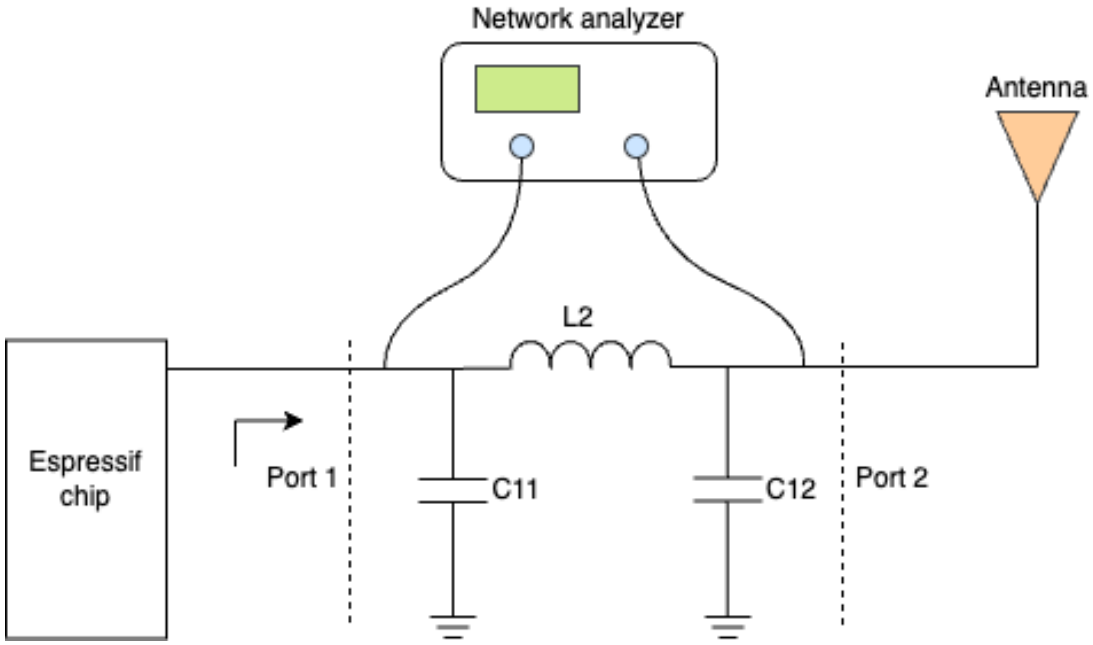

Fig. 6: ESP32-C61 RF Tuning Diagram

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, the transmission performance is best if the matching impedance is conjugate to the chip impedance. S21 is used to describe the transmission loss of signal from Port 1 to Port 2. If S11 is close to the chip conjugate point 35+j0 and S21 is less than -35 dB at 4.8 GHz and 7.2 GHz, the matching circuit can satisfy transmission requirements.

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter *PCB Layout Design*, you can refer to the value ranges in Table *Recommended Value Ranges for Components* to debug the matching circuit.

Table 4: Recommended Value Ranges for Components

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

Please use 0201 packages for RF matching components and add a stub to the first capacitor in the matching circuit at the chip end.

Note: If RF function is not required, it is recommended not to initialize the RF stack in firmware. In this case, the RF pin can be left floating. However, if RF function is enabled, make sure an antenna is connected. Operation without an antenna may result in unstable behavior or potential damage to the RF circuit.

1.3.7 UART

ESP32-C61 includes 3 UART interfaces, UART0, UART1, and UART2. U0TXD and U0RXD are GPIO11 and GPIO10 by default. Other UART signals can be mapped to any available GPIOs by software configurations.

Usually, UART0 is used as the serial port for download and log printing. For instructions on download over UART0, please refer to Section *Download Guidelines*. It is recommended to connect a 499 Ω series resistor to the U0TXD line to suppress harmonics.

If possible, use other UART interfaces as serial ports for communication. For these interfaces, it is suggested to add a series resistor to the TX line to suppress harmonics.

1.3.8 SPI

When using the SPI function, to improve EMC performance, add a series resistor (or ferrite bead) and a capacitor to ground on the SPI_CLK trace. If space allows, it is recommended to also add a series resistor and capacitor to ground on other SPI traces. Ensure that the RC/LC components are placed close to the pins of the chip or module.

1.3.9 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

GPIO7, GPIO8, GPIO9, MTMS, and MTDI are strapping pins.

All the information about strapping pins is covered in ESP32-C61 Series Datasheet > Chapter *Boot Configurations*.

In this section, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO8 and GPIO9 controls the boot mode. See Table *Boot Mode Control*.

Table 5: Boot Mode Control

Boot Mode	GPIO8	GPIO9
SPI Boot (default)	Any value	1
Joint Download Boot	1	0

Joint Download Boot supports the following download methods:

- USB-Serial-JTAG Download Boot

- UART Download Boot
- SPI Slave 2.0 Download Boot

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure *Setup and Hold Times for Strapping Pins* and Table *Description of Timing Parameters for Strapping Pins*.

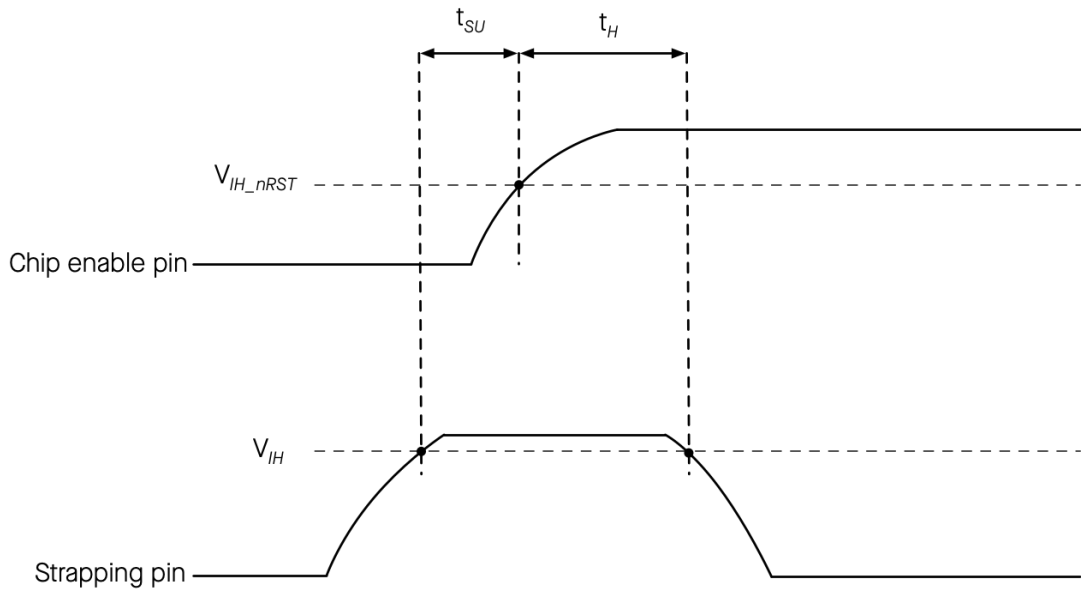

Fig. 7: Setup and Hold Times for Strapping Pins

Table 6: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_PU) is pulled high to activate the chip.	0
t_H	Time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

Attention:

- It is recommended to place a pull-up resistor at the GPIO9 pin.
- Do not add high-value capacitors at GPIO9, or the chip may enter download mode.

1.3.10 GPIO

The pins of ESP32-C61 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations (see ESP32-C61 Series Datasheet > Appendix *ESP32-C61 Consolidated Pin Overview*), whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP32-C61 Technical Reference Manual > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP32-C61 Series Datasheet > Section *Peripherals*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.

- Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in the table below. It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- Avoid using the pins already occupied by flash/PSRAM.
- In Deep-sleep mode, only LP GPIOs can be controlled, that is, the GPIOs whose power supply pin is VDDPST1 as listed in the table below.

Table 7: IO Pin Default Functions

Pin No	Pin Name	Pin Providing Power	At Reset	After Reset
6	XTAL_32K_P	VDDPST1		
7	XTAL_32K_N	VDDPST1		
8	GPIO2	VDDPST1		
9	MTMS	VDDPST1	IE	IE
10	MTDI	VDDPST1	IE	IE
11	MTCK	VDDPST1		IE
12	MTDO	VDDPST1		IE
13	SDIO_CMD	VDDPST2		IE
14	SDIO_CLK	VDDPST2		IE
15	SDIO_DATA0	VDDPST2		IE
16	SDIO_DATA1	VDDPST2		IE
17	SDIO_DATA2	VDDPST2		IE
18	SDIO_DATA3	VDDPST2		IE
19	SPICS1	VDD_SPI/VDDPST2		
20	SPICS0	VDD_SPI/VDDPST2		
22	SPIQ	VDD_SPI/VDDPST2		
23	SPIWP	VDD_SPI/VDDPST2		
24	VDD_SPI	VDDPST2		
25	SPIHD	VDD_SPI/VDDPST2		
26	SPICLK	VDD_SPI/VDDPST2		
27	SPID	VDD_SPI/VDDPST2		
28	USB_D-	VDDPST2		IE
29	USB_D+	VDDPST2	USB_PU	IE,USB_PU
30	GPIO24	VDDPST2		
31	GPIO8	VDDPST2	IE	IE
32	GPIO9	VDDPST2	IE,WPU	IE,WPU
33	U0RXD	VDDPST2		IE,WPU
34	U0TXD	VDDPST2		IE,WPU
35	GPIO29	VDDPST2		
36	GPIO7	VDDPST2	IE	IE

- IE –input enabled
- WPU –internal weak pull-up resistor enabled
- USB_PU –USB pull-up resistor enabled

1.3.11 ADC

Please add a 0.1 µF filter capacitor between ESP pins and ground when using the ADC function to improve accuracy.

ADC GPIOs are shown in the table below.

Table 8: ADC Functions

Pin No	IO Pin Name	ADC Function
7	XTAL_32K_N	ADC1_CH0
9	MTMS	ADC1_CH1
10	MTDI	ADC1_CH2
11	MTCK	ADC1_CH3

The calibrated ADC results after hardware calibration and software calibration are shown in the list below. For higher accuracy, you may implement your own calibration methods.

- When ATTEN=0 and the effective measurement range is 0 ~ 1000 mV, the total error is ±10 mV.
- When ATTEN=1 and the effective measurement range is 0 ~ 1300 mV, the total error is ±10 mV.
- When ATTEN=2 and the effective measurement range is 0 ~ 1900 mV, the total error is ±12 mV.
- When ATTEN=3 and the effective measurement range is 0 ~ 3300 mV, the total error is ±15 mV.

1.3.12 SDIO

ESP32-C61 series has only one SDIO slave controller that conforms to the industry-standard SDIO Specification Version 2.0. SDIO should be connected to specific GPIOs, namely SDIO_CMD, SDIO_CLK, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3. Please add a pull-up resistor to these GPIOs, and preferably reserve a series resistor on each trace.

1.3.13 USB

ESP32-C61 integrates a USB Serial/JTAG controller that supports USB 2.0 full-speed device.

GPIO12 and GPIO13 can be used as D- and D + of USB respectively. It is recommended to populate 22/33 ohm series resistors between the mentioned pins and the USB connector. Also, reserve a footprint for a capacitor to ground on each trace. Note that both components should be placed close to the chip.

The USB RC circuit is shown in Figure *ESP32-C61 USB RC Schematic*.

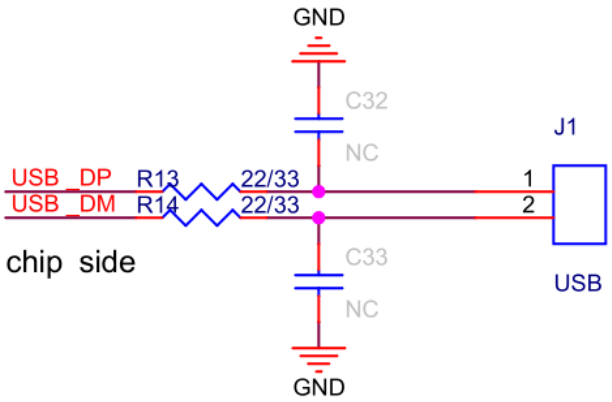

Fig. 8: ESP32-C61 USB RC Schematic

Note that upon power-up, the USB_D+ signal will fluctuate between high and low states. The high-level signal is relatively strong and requires a robust pull-down resistor to drive it low. Therefore, if you need a stable initial state, adding an external pull-up resistor is recommended to ensure a consistent high-level output voltage at startup.

ESP32-C61 also supports download functions and log message printing via USB. For details please refer to Section *Download Guidelines*.

1.4 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-C61 PCB layout using an ESP32-C61 module (see Figure *ESP32-C61 Reference PCB Layout*) as an example.

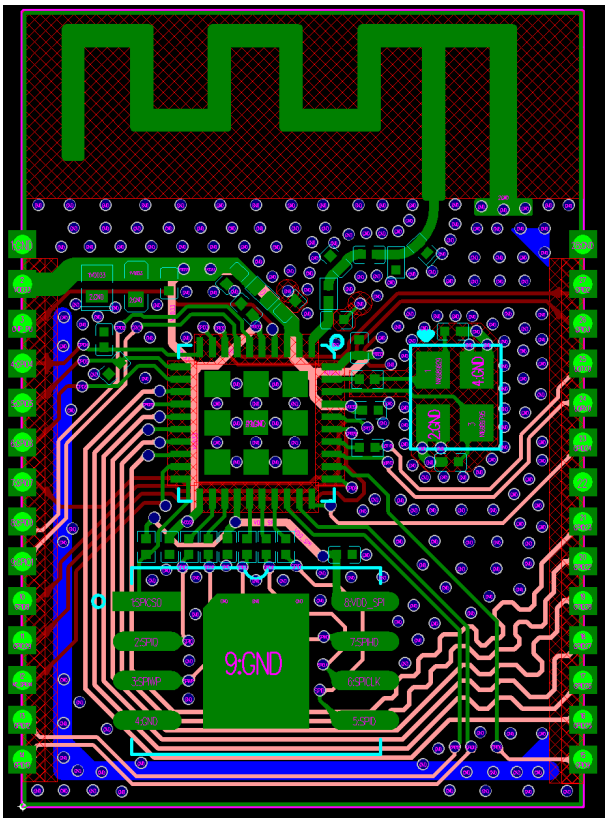

Fig. 9: ESP32-C61 Reference PCB Layout

1.4.1 General Principles of PCB Layout for the Chip

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

1.4.2 Power Supply

Four-Layer PCB Design

Figure *ESP32-C61 Power Traces in a Four-Layer PCB Design* shows the power traces in a four-layer PCB design.

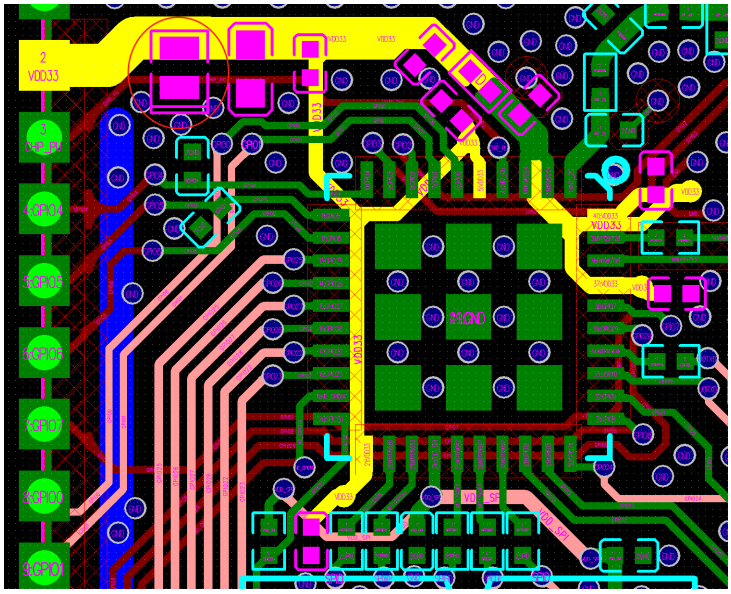

Fig. 10: ESP32-C61 Power Traces in a Four-Layer PCB Design

- A four-layer PCB design is recommended. Whenever possible, route the power traces on the inner layers (not the ground layer) and connect them to the chip pins through vias. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure *ESP32-C61 Power Traces in a Four-Layer PCB Design*. The width of the main power traces should be no less than 25 mil. The width of VDDA3 and VDDA4 at pin2 and pin3 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil. Ensure the power traces are surrounded by ground copper.
- The ESD protection diode is placed next to the power port (circled in red in Figure *ESP32-C61 Power Traces in a Four-Layer PCB Design*). The power trace should have a 10 µF capacitor on its way before entering into the chip. After that, the power traces are divided into several branches using a star-shaped topology, which reduces the coupling between different power pins.
- The power supply for pin2 and pin3 is RF related, so please place a 10 µF capacitor for each pin. You can also add a 0.1 µF or 1 µF capacitor in parallel.
- Add a CLC/LC filter circuit near pin2 and pin3 to suppress high-frequency harmonics.The power trace can be routed at a 45-degree angle to maintain distance from adjacent RF traces. Except for the 10 µF capacitor, it is recommended to use 0201 components. This allows the filter circuit for pin2 and pin3 to be placed closer to the pins, with a GND isolation layer separating them from surrounding RF and GPIO traces, while also maximizing the placement of ground vias. Using 0201 components enables placing a via to the bottom layer at the first capacitor near the chip, while maintaining a keep-out area on other layers, further reducing harmonic interference. See Figure *ESP32-C61 Power Traces for Pins 2 and 3*.

- Place appropriate decoupling capacitors at the rest of the power pins. Ground vias should be added close to the capacitor’ s ground pad to ensure a short return path.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- The ground pads of the chip and surrounding circuit components should make full contact with the ground copper pour rather than being connected via traces.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure *ESP32-C61 Power Traces in a Four-Layer PCB Design*. This helps effectively reduce solder leakage issues when soldering the module EPAD to the substrate.

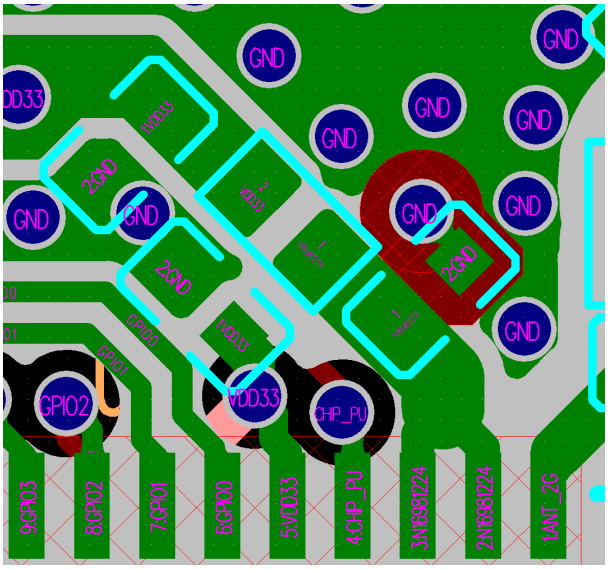

Fig. 11: ESP32-C61 Power Traces for Pins 2 and 3

Two-Layer PCB Design

Figure *ESP32 Power Traces in a Two-Layer PCB Design* shows the power traces in a two-layer PCB design.

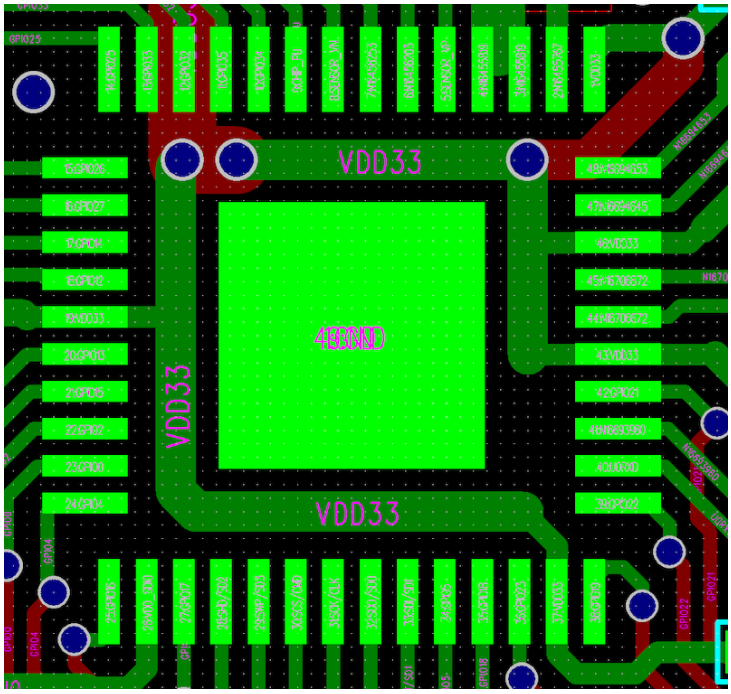

Fig. 12: ESP32 Power Traces in a Two-Layer PCB Design

- For a two-layer design, ensure to provide a continuous reference ground for the chip, RF, and crystal oscillator, as shown in the figure above.
- In the figure above, the trace VDD33 represents the 3.3 V power trace. Unlike a four-layer design, the power trace should be routed on the top layer as much as possible. Therefore, the thermal pad in the center of the chip should be reduced in size, allowing the power trace to pass between the signal pads and the thermal pad. Vias to the bottom layer should only be used when absolutely necessary.

- Other layout considerations are the same as for a four-layer design.
- Note that there are no official two-layer modules. The figure above uses the ESP32 module as an example.

1.4.3 Crystal

Figure *ESP32-C61 Crystal Layout (with Keep-out Area on Top Layer)* shows a reference PCB layout where the crystal is connected to the ground through vias and a keep-out area is maintained around the crystal on the top layer for ground isolation.

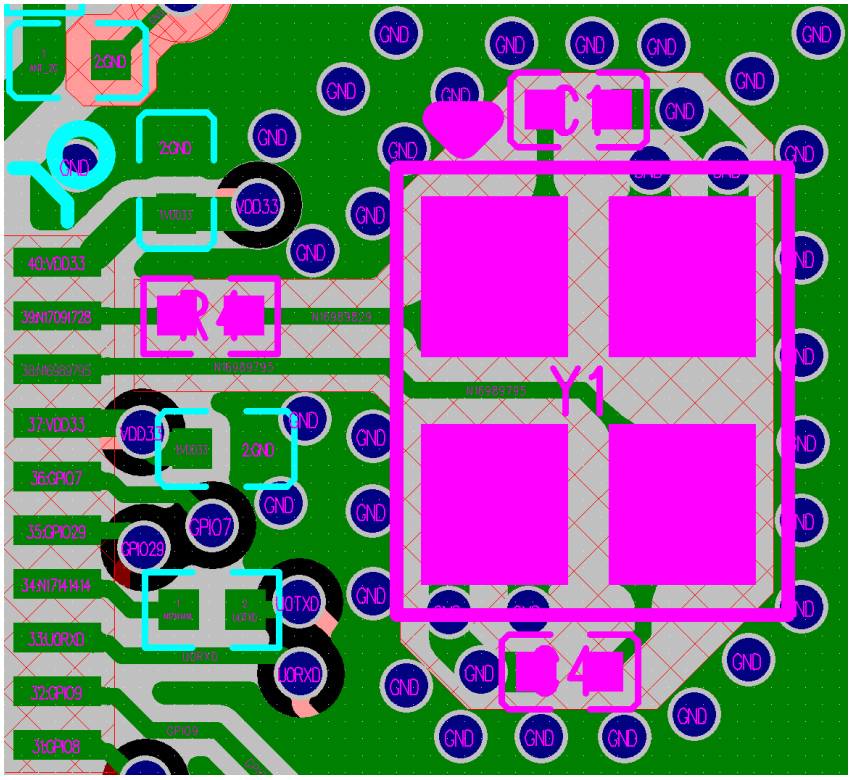

Fig. 13: ESP32-C61 Crystal Layout (with Keep-out Area on Top Layer)

If there is sufficient ground on the top layer, it is recommended to maintain a keep-out area around the crystal for ground isolation. This helps to reduce the value of parasitic capacitance and suppress temperature conduction, which can otherwise affect the frequency offset. If there is no sufficient ground, do not maintain any keep-out area.

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.4 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces.
- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by ground copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

1.4.4 RF

The RF trace is routed as shown highlighted in pink in Figure *ESP32-C61 RF Layout in a Four-layer PCB Design*.

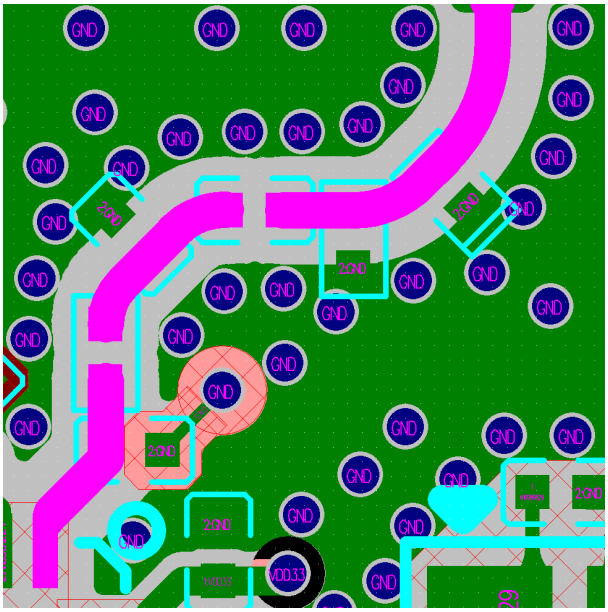

Fig. 14: ESP32-C61 RF Layout in a Four-layer PCB Design

The RF layout should meet the following guidelines:

- The RF trace should have a 50 Ω characteristic impedance. The reference plane is the layer next to the chip. For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown below.

- A CLCCL matching circuit should be added to the RF trace. Please use 0201 components and place them close to the pin in a zigzag. In other words, the two capacitors should not be oriented in the same direction to minimize interference.
- Add a stub on the grounding capacitor near the chip side in the CLCCL matching circuit to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in figure below is the stub. Note that a stub is not required for package types of 0402 and above.
- It is recommended to keep all layers clear under the IPEX antenna connector. See Figure *ESP32-C61 IPEX Layout*.
- For PCB antennas, make sure to validate them through both simulation and real-world testing on a development board. It is recommended to include an additional CLC matching circuit for antenna tuning. Place this circuit as close to the antenna as possible.

- The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
CM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8.22	4.6
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.6
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8.22	4.6
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Fig. 15: ESP32-C61 PCB Stack-up Design

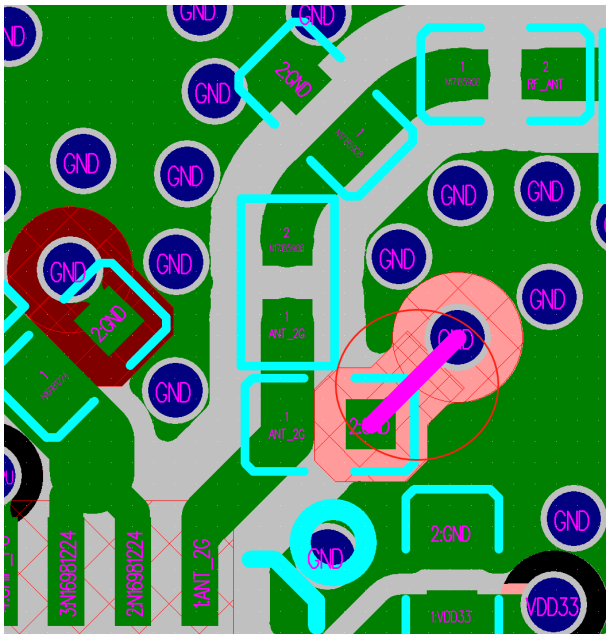

Fig. 16: ESP32-C61 Stub in a Four-layer PCB Design

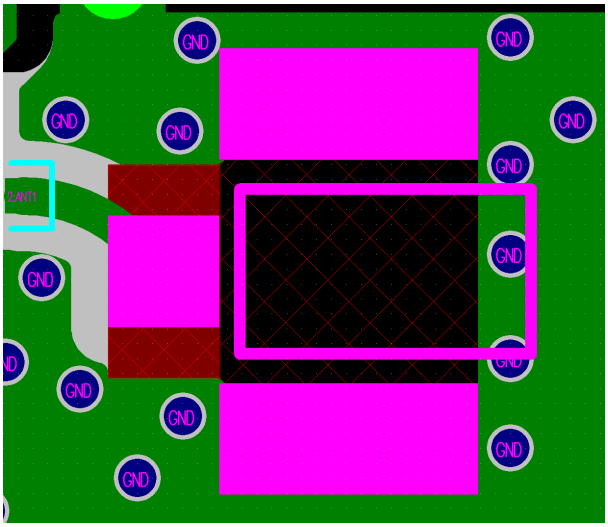

Fig. 17: ESP32-C61 IPEX Layout

1.4.5 Flash and PSRAM

The layout for flash should follow the guidelines below:

- Place the zero-ohm resistors in series on the SPI lines close to ESP32-C61.
- Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately.
- If the flash and PSRAM are located far from ESP32-C61, it is recommended to place appropriate decoupling capacitors both at VDD_SPI and near the flash and PSRAM power supply.

Figure *ESP32-C61 Quad SPI Flash Layout* shows the quad SPI flash layout.

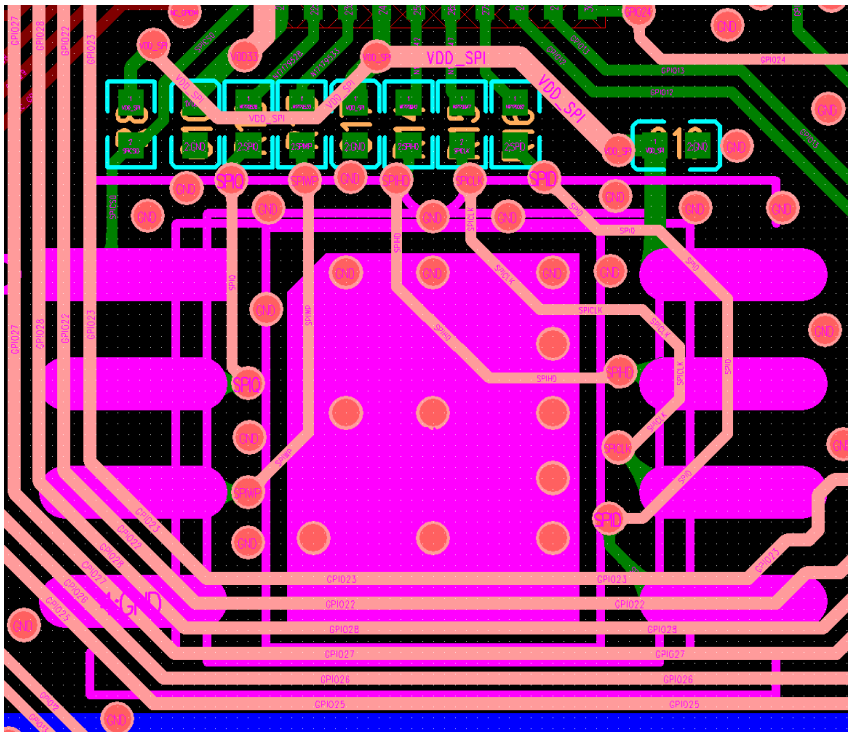

Fig. 18: ESP32-C61 Quad SPI Flash Layout

1.4.6 UART

Figure *ESP32-C61 UART Layout* shows the UART layout.

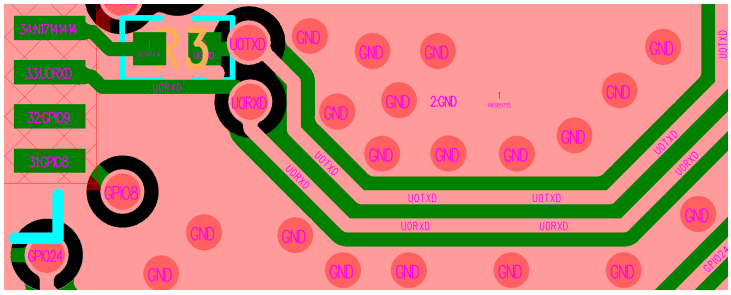

Fig. 19: ESP32-C61 UART Layout

The UART layout should meet the following guidelines:

- The series resistor on the U0TXD trace needs to be placed close to the chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

1.4.7 General Principles of PCB Layout for Modules (Positioning a Module on a Base Board)

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the baseboard on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna close to the edge of the base board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

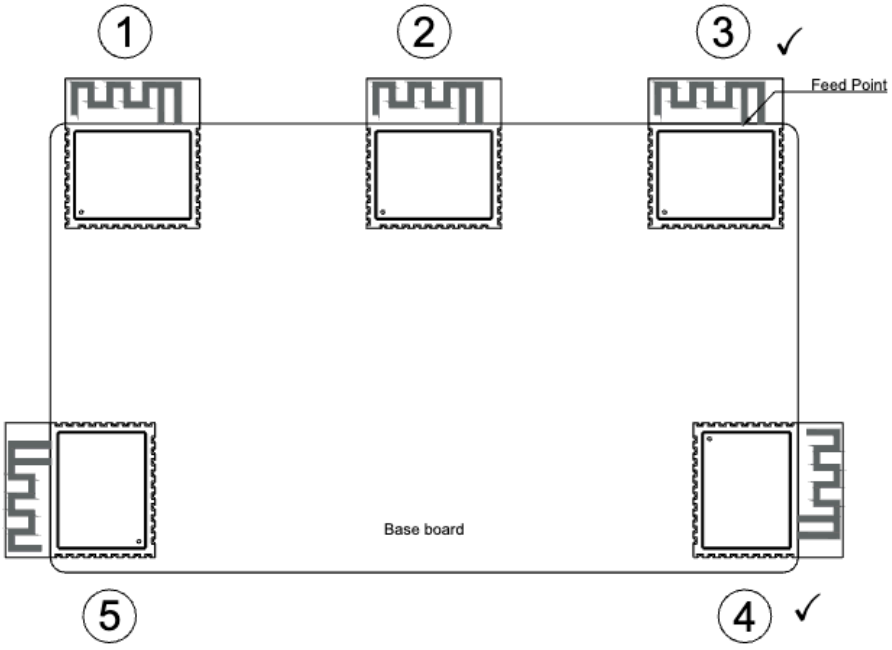

Fig. 20: Placement of ESP32-C61 Modules on Base Board (antenna feed point on the right)

If the PCB antenna cannot be placed outside the board, please ensure a clearance of at least 15 mm (in all directions) around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest

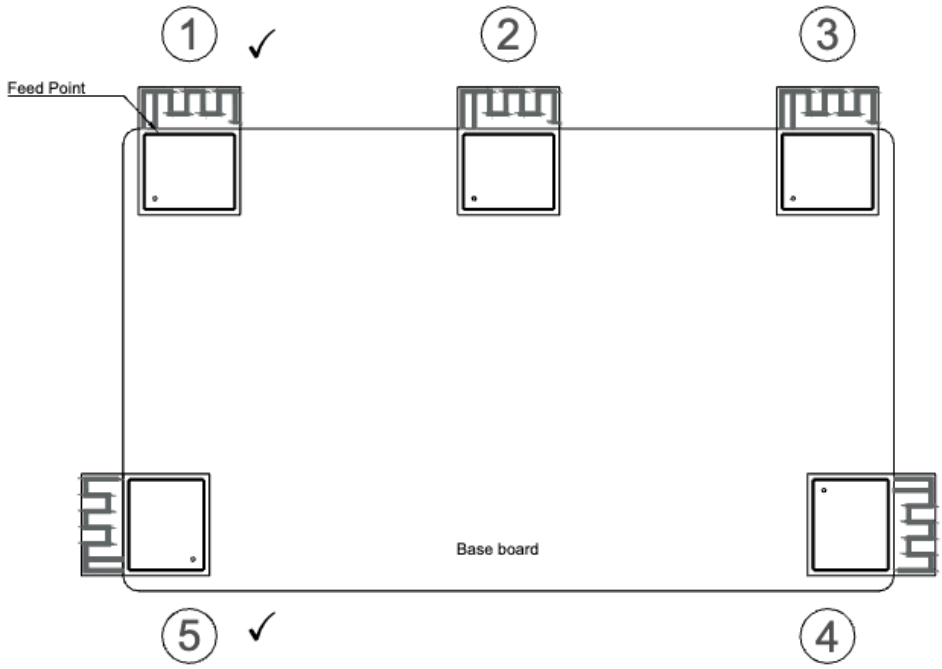

Fig. 21: Placement of ESP32-C61 Modules on Base Board (antenna feed point on the left)

to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure *Keepout Zone for ESP32-C61 Module's Antenna on the Base Board* shows the suggested clearance for modules whose antenna feed point is on the right.

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification. It is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

1.4.8 USB

The USB layout should meet the following guidelines:

- Reserve space for resistors and capacitors on the USB traces close to the chip side.
- Use differential pairs and route them in parallel at equal lengths. Maintain a differential pair impedance of 90 Ω with a tolerance of ±10%.
- USB differential traces should minimize via transitions as much as possible to ensure better impedance control and avoid signal reflections. If vias are necessary, add a pair of ground return vias at each transition point.
- Ensure there is a continuous reference layer (a ground layer is recommended) beneath the USB traces.
- Surround the USB traces with ground copper.

1.4.9 SDIO

The SDIO layout should follow the guidelines below:

- Minimize parasitic capacitance of SDIO traces as they involve high-speed signals.
- The trace lengths for SDIO_CMD and SDIO_DATA0 ~ SDIO_DATA3 should be within ± 50 mil of the SDIO_CLK trace length. Use serpentine routing if necessary.
- For SDIO routing, maintain a 50 Ω single-ended impedance with a tolerance of ±10%.
- Keep the total trace length from SDIO GPIOs to the master SDIO interface as short as possible, ideally within 2000 mil.

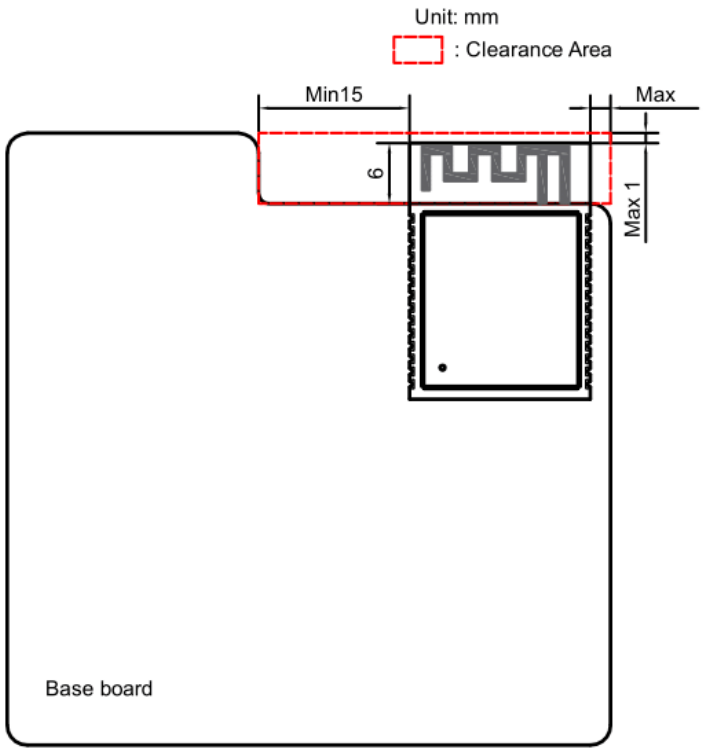

Fig. 22: Keepout Zone for ESP32-C61 Module' s Antenna on the Base Board

- Ensure that SDIO traces do not cross layers. Besides, a reference plane (preferably a ground plane) must be placed beneath the traces, and continuity of the reference plane must be ensured.
- It is recommended to surround the SDIO_CLK trace with ground copper.
- For multi-layer PCB designs, it is recommended to route the SDIO traces to the inner layers immediately after exiting the chip through vias, in order to reduce interference on high-speed signal lines. Additionally, place a pair of ground vias near the layer transition to ensure proper return path.

1.4.10 Typical Layout Problems and Solutions

When ESP32-C61 sends data packages, the voltage ripple is small, but RF TX performance is poor.

Analysis: The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution: This problem is caused by improper layout for the crystal and can be solved by re-layout. Please refer to Section *Crystal* for details.

When ESP32-C61 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis: The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution: Match the antenna' s impedance with the π-type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

TX performance is not bad, but the RX sensitivity is low.

Analysis: Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution: Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please refer to Section *RF* for details.

1.5 Download Guidelines

You can download firmware to ESP32-C61 via UART and USB.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, according to Table *Boot Mode Control*.
2. Power up the chip or module and check the log via the UART0 serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using the Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. If the flash is empty, set the chip or module to Joint Download Boot mode, according to Table *Boot Mode Control*.
2. Power up the chip or module and check the log via USB serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via USB using Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.
6. If the flash is not empty, start directly from Step 3.

Note:

- For firmware download instructions, see also ESP Product Firmware Download Instructions.
- For how to check serial port output, see also Establish Serial Connection with ESP32-C61.
- It is advised to download the firmware only after the "waiting for download" log shows via the serial port.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one COM port.
- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip or module to Joint Download Boot mode first by configuring the strapping pin.
  - USB PHY is disabled by the application;
  - USB is secondary developed for other USB functions, e.g., USB host, USB standard device;
  - USB IOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.

1.6 Related Documentation and Resources

1.6.1 ESP32-C61 Modules

For a list of ESP32-C61 modules please check the Modules section on Espressif's official website.

For module reference designs please refer to:

- Download links

The above reference design applies only to the specified MPN. If a different MPN is used, the corresponding BOM and schematic may vary. Please refer to the relevant datasheet and design guide to obtain the correct design information.

The antenna design is for reference only. For actual projects, perform antenna simulations based on the PCB layout.

Note: Use the following tools to open the files in module reference designs:

- .DSN files: OrCAD Capture V16.6
- .pcb files: Pads Layout VX.2. If you cannot open the .pcb files, please try importing the .asc files into your software to view the PCB layout.

1.6.2 ESP32-C61 Development Boards

For a list of the latest designs of ESP32-C61 boards please check the Development Boards section on Espressif's official website.

1.6.3 Other Related Documentation and Resources

- Chip Datasheet (PDF)
- Technical Reference Manual (PDF)
- ESP32-C61 Chip Variants
- Espressif KiCad Library
- ESP Product Selector
- Regulatory Certificates
- User Forum (Hardware)
- Technical Support
- ESP-FAQ

1.7 Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor acts as a placeholder in the circuit, allowing for the replacement with a higher-ohm resistor based on specific design requirements.

1.8 Revision History

Table 9: Revision History

Date	Version	Release Notes
2025-08-19	v1.0	First release of ESP32-C61 Hardware Design Guidelines.

1.9 Disclaimer and Copyright Notice

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